A 9-16 GHZ MONOLITHIC HEMT LOW NOISE AMPLIFIER WITH EMBEDDED LIMITERS

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Abstract

A novel 9 - 16 GHz monolithic HEMT low noise amplifier with on-chip limiters has been designed, fabricated, and measured. This paper presents the design topology, the new fabrication technology, and the on-wafer measurements of this circuit. The limiter consists of one PIN diode and one Schottky diode. The low noise amplifier itself is a single stage balanced amplifier with one limiter embedded in each single-ended amplifier.

Introduction

A high power diode limiter is usually required in the front-end module to protect active devices in the low noise amplifiers from high rf input power levels. Traditionally, the limiters have always been MIC which not only take up a large area but also have high insertion loss. A new fabrication technology has been successfully developed at TRW which allows high electron mobility transistors (HEMT), PIN diodes, and Schottky diodes to be monolithically grown and processed on the same wafer.

A 3 to 16 GHz MMIC limiter was designed and fabricated using this new process. With one PIN diode and one Schottky diode, the limiter has less than 0.6 dB of insertion loss throughout the band of interest. In addition, it can sustain 30 dBm of CW input power with ~10 dB of isolation. A 9 to 16 GHz low noise amplifier which has been designed and fabricated by the standard low noise HEMT process previously was fabricated by this new process. The measured noise figure is less than 1.8 dB which is comparable to the standard low-noise HEMT process.

With the success of the MMIC limiters and MMIC LNAs processed by this new fabrication technology, a further step was taken to integrate the limiter and the LNA into one single MMIC chip. The 9 - 16 GHz LNA with embedded limiters described in this paper demonstrates the validity of the design and the combined PIN/HEMT process.

Fabrication and Circuit Design

The fabrication for the PIN/HEMT circuits is performed using a selective epitaxial growth technique on 3-inch undoped GaAs substrates. The optimized PIN diode epitaxial structure is grown first, and then followed by process definition of the PIN diode and HEMT active regions. A second epitaxial growth of pseudomorphic InGaAs HEMT material is done and the complete PIN/HEMT process follows using the merged process which consists of the baseline 0.2 μm T-gate low noise HEMT process [1], and the Schottky, base mesa and p-ohmic steps necessary to create the limiters.

The PIN diode and Schottky diode sizes are the important elements to determine the survivability levels and the insertion loss of limiters. With one limiter embedded in each single stage amplifier and the amplifiers combined by a pair of Lange couplers on the input and output, the diodes will only need to survive half of the maximum required input power levels that a stand-alone limiter would otherwise need to survive to. Another major advantage of having the limiter embedded inside the Lange couplers is that the diode parasitics can be absorbed into the noise matching circuits to the devices. Thus, the extra noise figure contributed by the limiter itself can be minimized and the overall noise figure of the complete LNA can be kept to a minimum. The complete circuit schematic is shown in figure 1. The HEMT devices used are 4-finger and 150 μm device width. The PIN diode and Schottky diode used in the limiter are 15 μm radius and 10 μm radius, respectively.

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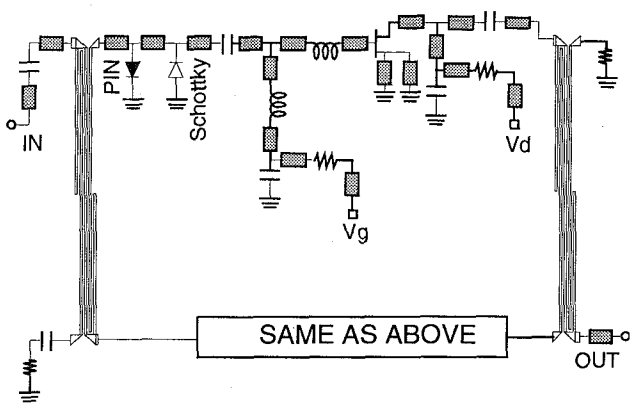

Fig. 1 Circuit schematic of 9 - 16 GHz low noise amplifier with embedded limiters

Performance

The completed LNA / limiter MMIC chip measures 3800 μm by 3200 μm in size which is the same as the stand alone LNA MMIC. Figure 2 shows the on-wafer s-parameters and noise figures tests data of the chip. The LNA has 12 dB of gain and less than 2.2 dB of noise figure across the band of interest (9 - 16 GHz). A survivability test was also done on the chip and the Pin vs. Pout data is shown in Fig. 3. The LNA is able to handle at least 30 dBm of CW input power at 12.5 GHz without failing as demonstrated by the small signal gain measured after the circuit was measured at each input power level.

Another design that is a single limiter in series with a balanced LNA was also done. The limiter in this chip also consists of one PIN diode and one Schottky diode. The size of the PIN diode is larger than the one used in the embedded design because the limiter must now sustain the high rf input power directly. Although the chip can also survive to more than 30 dBm of CW input power and it only requires one limiter, the noise figure of this series design is about 0.2 - 0.3 dB higher than the embedded design.

A MMIC limiter has also been designed and fabricated. The limiter uses one PIN diode of 14 μm radius and one Schottky diode of 8 μm radius and the limiter chip measures 1266 μm by 1200 μm in size. The measured insertion loss of the limiter is about 0.6 dB at 16 GHz. A 9 - 16 GHz MMIC LNA without a limiter has also been designed and fabricated by the same fabrication process. It has the same HEMT devices periphery and similar input and output matching circuits. This circuit exhibited < 1.8 dB noise figure and higher than 12 dB gain.

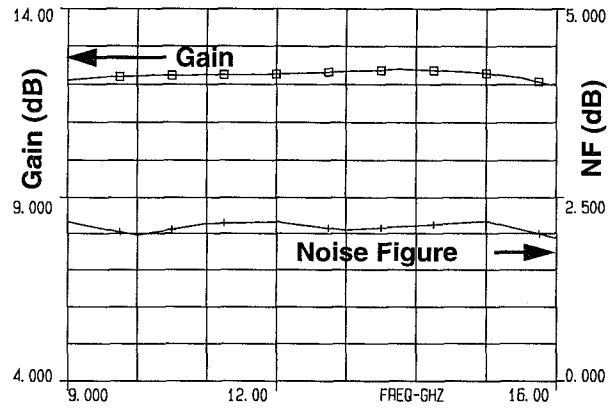

Fig. 2 On-wafer measurements of S-parameters and Noise Figure.

Conclusion

We have demonstrated a MMIC design that incorporates limiter and LNA into one single chip without increasing the total chip size. Among the three approaches to combine limiter and LNA, this design has shown the best noise figure performance. Furthermore, high survivability level (> 30 dBm CW) has also been demonstrated. In summary, it has been proven that a limiter can be inserted into a front-end module without degrading the noise figure very much or increasing the module size.

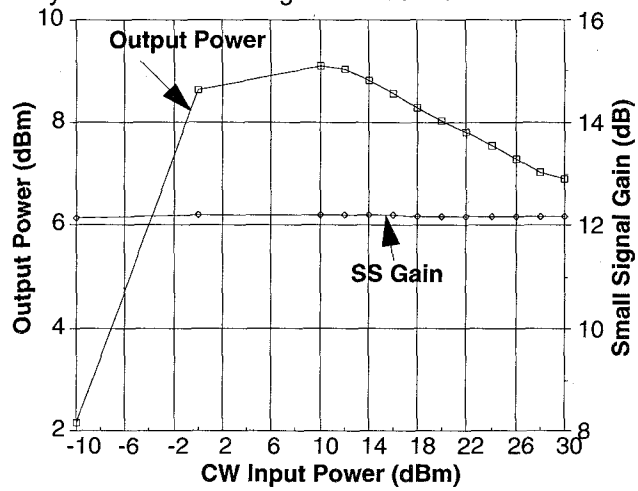

Fig. 3 On-wafer Pin vs. Pout measurement at 12 GHz

References

[1] B. Nelson, et. al., "Octave Band InGaAs HEMT MMIC Low Noise Amplifiers to 40 GHz," 12th Annual IEEE GaAs IC Symposium, New Orleans, LA, Oct. 7-10, 1990, pp.165-168.